**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (previously presented): A method of correcting critical dimensions of line patterns on a wafer, the method comprising:

providing line width deviation data of transferred line patterns, the line width deviation comprising a deviation of an after-etch-inspection critical dimension of the transferred line patterns onto the wafer;

executing an inspection program to classify line patterns of a mask layout into at least a first-type line pattern and a second-type line pattern according to the line width deviation data of the transferred line patterns;

making a line width correction of a first constant value on the first-type line pattern and making a line width correction of a second constant value on the second-type line pattern; and

transferring the line patterns of the corrected mask layout to the wafer.

Claim 2 (original): The method of claim 1 wherein a pattern density of the first-type line pattern is different from a pattern density of the second-type line pattern.

Claim 3 (original): The method of claim 2 wherein the pattern density is determined by a distance between two adjacent line patterns.

Claim 4 (original): The method of claim 1 wherein the line width deviation is a result of a systematic error.

Claim 5(original): The method of claim 1 wherein the line width deviation is a result of a micro-loading effect.

Claim 6 (canceled)

Claim 7 (original): The method of claim 1 wherein the first-type line pattern comprises dense patterns or semi-dense patterns, and the second-type line pattern comprises isolated patterns.

Claim 8 (original): The method of claim 1 wherein the first-type line pattern comprises isolated patterns or semi-isolated patterns, and the second-type line pattern comprises dense patterns.

Claim 9 (original): The method of claim 1 wherein the line width correction of the first constant value and the line width correction of the second constant value comprise increasing line widths of the line patterns or decreasing the line widths of the line patterns.

Claim 10 (original): The method of claim 1 wherein each of the line patterns is used for defining a conductive area.

Claim 11 (previously presented): A method of correcting critical dimensions of element patterns on a wafer, the method comprising:

providing pattern deviation data of transferred element patterns, the pattern deviation comprising a deviation of an after-etch-inspection critical dimension of the transferred element patterns onto the wafer;

executing an inspection program to classify element patterns of a mask layout into at least a first-type element pattern and a second-type element pattern according to the

pattern deviation data of the transferred element patterns;

making a selective correction on the first-type element pattern and the second-type element pattern, respectively; and

transferring the element patterns of the corrected mask layout to the wafer.

Claim 12 (previously presented): The method of claim 11 wherein the element patterns comprise line patterns.

Claim 13 (canceled)

Claim 14 (previously presented): The method of claim 12 wherein the selective correction comprises increasing line widths of the line patterns or decreasing the line widths of the line patterns.

Claim 15 (previously presented): The method of claim 11 wherein the pattern deviation is a result of a systematic error.

Claim 16 (previously presented): The method of claim 11 wherein the pattern deviation is a result of a micro-loading effect.

Claim 17 (canceled)

Claim 18 (previously presented): The method of claim 11 wherein the first-type element pattern comprises dense patterns or semi-dense patterns, and the second-type element pattern comprises isolated patterns.

Claim 19 (previously presented): The method of claim 11 wherein the

first-type element pattern comprises isolated patterns or semi-isolated patterns, and the second-type element pattern comprises dense patterns.

Claim 20 (previously presented): The method of claim 11 wherein each of the element patterns is used to define a conductive area.

Claims 21-29 (canceled)